Jointly Organized by
Electronics & ICT Academy

IIT Guwahati , NIT Patna, IIITDM Jabalpur & MNIT Jaipur
http://www.mnit.ac.in/eict

Online mode Programme
on
Digital CMOS Circuit Design

June 22- July 3, 2026
(4 hours/day)

Faculty Development Programme
Electronics & ICT Academy under aegis of

Ministry of Electronics and Information Technology
Government of India

meity.gov.in/content/schemes-projects

Chairman, EICT Academy & Director MNIT Jaipur
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Objective (Electronics & ICT Academy-Phase II)
1)To conduct specialized FDPs for faculty/mentor training in line with the vision of MeitY by promoting emerging areas of technology and other high-priority areas that are pillars of both the "Make in India" and the "Digital India" programs.
2) To promote synergy and collaboration with industry, academia, universities and other institutions of learning, especially in emerging technology areas.
3) To support the National Policy on Electronics 2019 (NPE 2019) which envisions positioning India as a global hub for ESDM sector, including MeitY Schemes/policies such as Programme for Semiconductors and Display Fab Ecosystem; India AI; National Programme on AI, Production Linked Incentive Scheme for IT Hardware & Large-Scale Electronics Manufacturing; EMC; SPECS; Chips to System (C2S); etc.
4) To promote standardization of FDPs through Joint Faculty Development Programmes.
5) To support the vision of the National Education Policy (NEP 2020), which mandates that Indian educators go through at least 50 hours in professional development programmes per year.
6) To design, develop & deliver specialised FDPs on emerging technologies/ niche areas/ specialised modules for specific research areas for Faculty in Higher Education Institutions (HEI), besides FDPs on multi-disciplinary areas connected with ICT tools and technologies and other digital hybrid domains, covering a wide spectrum of engineering and non-engineering colleges, polytechnics, ITIs, and PGT educators.

An intensive 40 Hours Training Programme in online mode is being organized for faculty and doctoral students of engineering and technological institutions. It is also open to working professionals from industry/organizations. The main theme of training program will be oriented around exploring the state of the art methods for VLSI Design & Technology.

Experts/Speakers-

Speakers are from IITs, NITs, and IIITs, and industry experts from IBM.

Programme Modules:

Module 1: Inauguration, Key Note Lecture, Logic Gates (AND, OR, NOT etc.), Boolean Algebra, Verification and interpretation of truth table for various gates, Realization of logic functions with the help of universal gates.
Module 2: Gate level combinational circuits: Mux/Demux, Encoder/Decoder, Adder/Subtractor, Boolean functions using MUX, Design of MUX and DEMUX using universal logic gates, Decoder/De-multiplexer and encoder using logic gates, Comparator, Parity generators, Half adder using basic and universal gates, Half and Full Subtractor, One-bit and two-bit comparator using logic gates, BCD to 7 Segment LED display decoder.
Module 3: Gate level sequential circuits: Latches, Flip-flops (RS, JK, D, T, Master Slave), NOR gate latch, JK Flip-Flop, Truth table of RS, JK, T and D flip-flops, Registers, Shift Register.
Module 4: Counters: Ripple and Ring, Shift Register and Counters, Two-bit ripple counter, Synchronous up-down counter.
Module 5: Design of synchronous sequential finite state machine, Analysis of synchronous sequential finite state machine.

Programme Coordinator:

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Dr. Menka Yadav, MNIT Jaipur		954 965 0791
		SCAN QR Code to Register

Registration:
Registration is open to faculty, working professionals, industry persons, doctoral, postgraduate and graduate students from India and rest of the world. Participants will be admitted on first-come first-served basis. **Register online at** (http://online.mnit.ac.in)

Mode of programme	Academia (faculty/Students): India/SAARC/Africa	Others: India/SAARC/Africa	Rest of the world
Online	Rs. 500/-	Rs. 1000/-	US $ 60/-

(A) Fee once paid will not be refunded back.
(B) The fee covers online participation in the programme, tutorial notes and examination, certification charges etc.
(C) The registration amount may be paid through online mode - NEFT / UPI / Cards / SWIFT, provided at the registration portal.
(D) Detailed schedule will be shared after receiving registration form.
→ For queries,**email us at** fdp.academy@mnit.ac.in

MNIT Jaipur one of the oldest NITs, the institute has a rich heritage of sixty years producing world class engineers, managers, architects and scientists. Ranked 43rd nationally in the NIRF ranking-2024 (Engineering), the institute offers learning opportunities for undergraduate, postgraduate students, and researchers in various domains. Having a lush green campus of over 317 acres within the heart of the pink city, close to Jaipur International Airport, the campus offers a safe and lively environment. A world class teaching infrastructure, state-of-art laboratories welcome you at the campus. The institute has a vision to impart education of international standards and conduct research at the cutting edge of